

APPLICATION NOTES FROM: INTELLUX INCORPORATED, 26 COROMAR DRIVE, GOLETA, CALIFORNIA (805) 968-3541

The functional flexibility of the Intellux Hybrid Microcircuit is demonstrated by the high voltage dual relay driver, RD 1513N which features operation at 30 VDC positive.

PERFORMANCE:	Max. operating voltage	+30 VDC
	Max. output current (each driver)	300 ma
	Typical noise immunity:	
	Off state	6 volts min.
	On state	5 volts min.

Note: Environmental specifications, physical data, and installation diagrams are identical to those for the Intellux series HV microcircuits.

Pricing is available from Intellux or your local representative.

The basic circuit of a relay driver is shown on Fig. 1. The transistor Q acts as a switch, connecting or disconnecting the relay coil from the DC power supply.

The switch is opened or closed by the input signal V_{IN} . When the input signal is 0 volts (grounded) or negative, the switch is open. When the input signal is positive and of sufficiently high amplitude the switch closes and the relay coil is energized.

The steady state current flowing through the relay coil is

$$I_r = \frac{V_{CC} - V_{CE\ sat}}{R_r} \quad (\text{Amps}) \quad (1)$$

When the transistor (switch) Q is fully saturated, the collector-emitter voltage $V_{CE\ sat}$ is very low (typically 0.2 v) and can be omitted. Hence:

$$I_r \approx \frac{V_{CC}}{R_r} \quad (\text{Amps}) \quad (2)$$

For safe operation this steady state current I_r must be smaller than the maximum rated current of the transistor Q for the max ambient temperature at which the unit will operate.

The steady state input current I_{IN} required to saturate the transistor can be calculated from the equation:

$$I_{IN} = \frac{I_r}{h_{FE}} \quad (\text{Amps}) \quad (3)$$

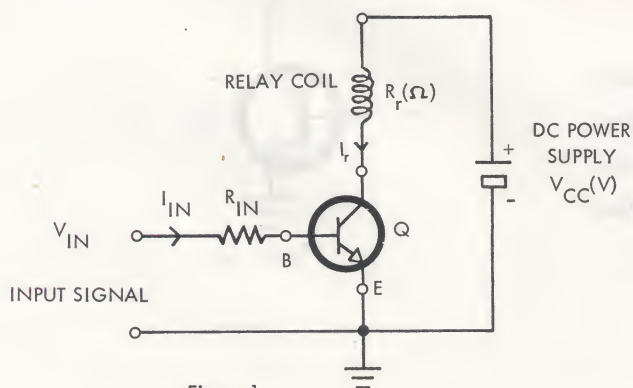


Figure 1

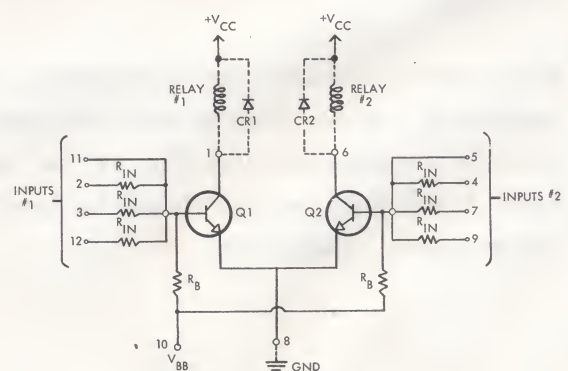


Figure 2

And the input voltage required is

$$V_{IN} = I_{IN}R_{IN} + V_{BE \text{ sat}} \quad (V) \quad (4)$$

Substituting equations (2) and (3) in (4) and rearranging:

$$R_{IN} = h_{FE}R_r \frac{V_{IN} - V_{BE \text{ sat}}}{V_{CC}} \quad (\Omega) \quad (5)$$

In applications where the input voltage V_{IN} is approximately equal to the power supply voltage V_{CC} and neglecting $V_{BE \text{ sat}}$ we get:

$$R_{IN} \approx h_{FE}R_r \quad (\Omega) \quad (6)$$

which means that the input resistor of the relay driver should be approximately equal to h_{FE} times the resistance of the relay coil R_r .

In the Intellux relay driver module there are three input resistors designated R_{IN} connected to the base of each of the two switching transistors. (See Fig. 2)

These resistors can be connected in parallel to obtain 3 different values of input resistance namely:

$$\begin{aligned} R_{IN} &= 6.8 \text{ K (one resistor only)} \\ \frac{R_{IN}}{2} &= 3.4 \text{ K (2 resistors in parallel)} \\ \frac{R_{IN}}{3} &= 2.27 \text{ K (3 resistors in parallel)} \end{aligned}$$

Direct connections to the bases (pins #11 and #5) are also provided so that an external resistor smaller than 2.2K can be used, if required.

Base bias resistors R_B are available to connect to a small negative voltage for operation at high temperatures or to improve the noise immunity of the unit.

The high speed diodes CR1 and CR2 should always be used in parallel with the relays to protect the transistors from high voltage transients due to rapid switching.

If the diode slows down the de-energizing of the relay excessively, a Zener diode in series with the switching diode is recommended. (See Fig. 3.) The value of the Zener break-down voltage should be lower than the power supply voltage V_{CC} .

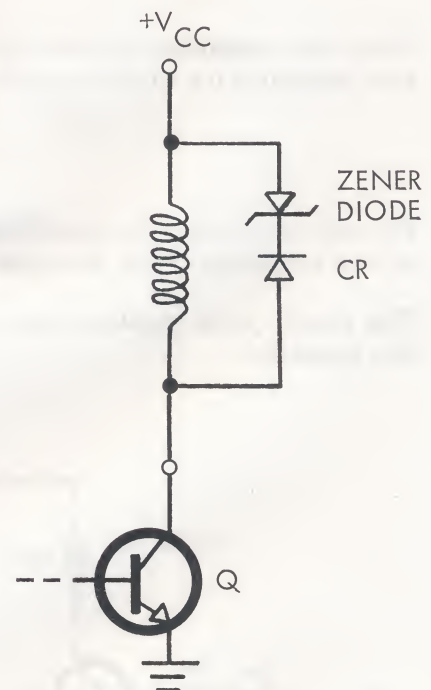


Figure 3.

INTELLUX INCORPORATED, SANTA BARBARA RESEARCH PARK, 26 COROMAR DRIVE, GOLETA, CALIFORNIA, PHONE (805) 968-3541, CABLE: INTLUX

This subsystem, consisting of Intellux hybrid microcircuits, may be used to drive four-lead stepping motors of the "bifilar" or "wave" type. Such motors are widely used in incremental tape transports, and are characterized by the requirement for outputs from a two-bit Gray code generator

Figure 1 shows a generator arranged in the form of a two-stage "twisted" ring counter. In Figure 1A the twist occurs between the output of FFB and the input to FFA. The Table of Output States corresponding to such an arrangement describes the stepping sequence required for forward rotation. Figure 1B shows the same circuit with the twist between the output of FFA and the input to FFB. Its Table of Output States defines the requirement for reverse rotation.

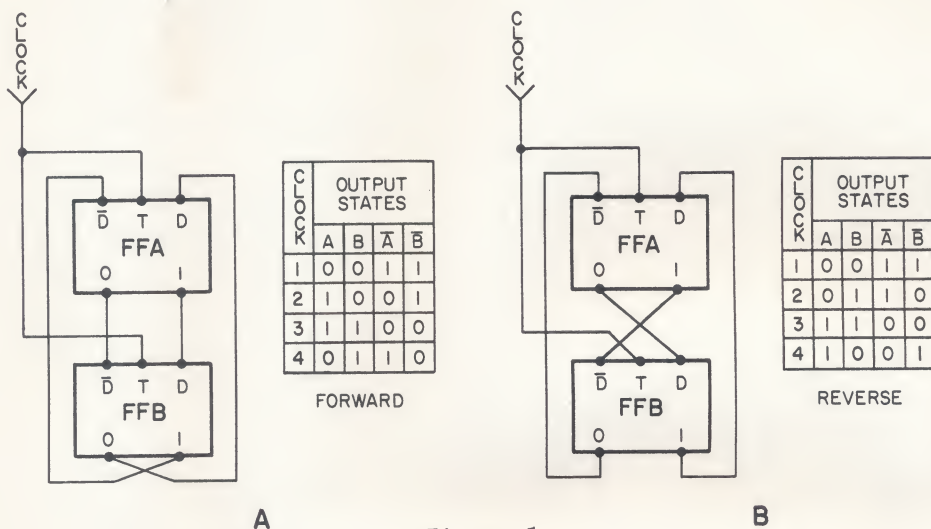
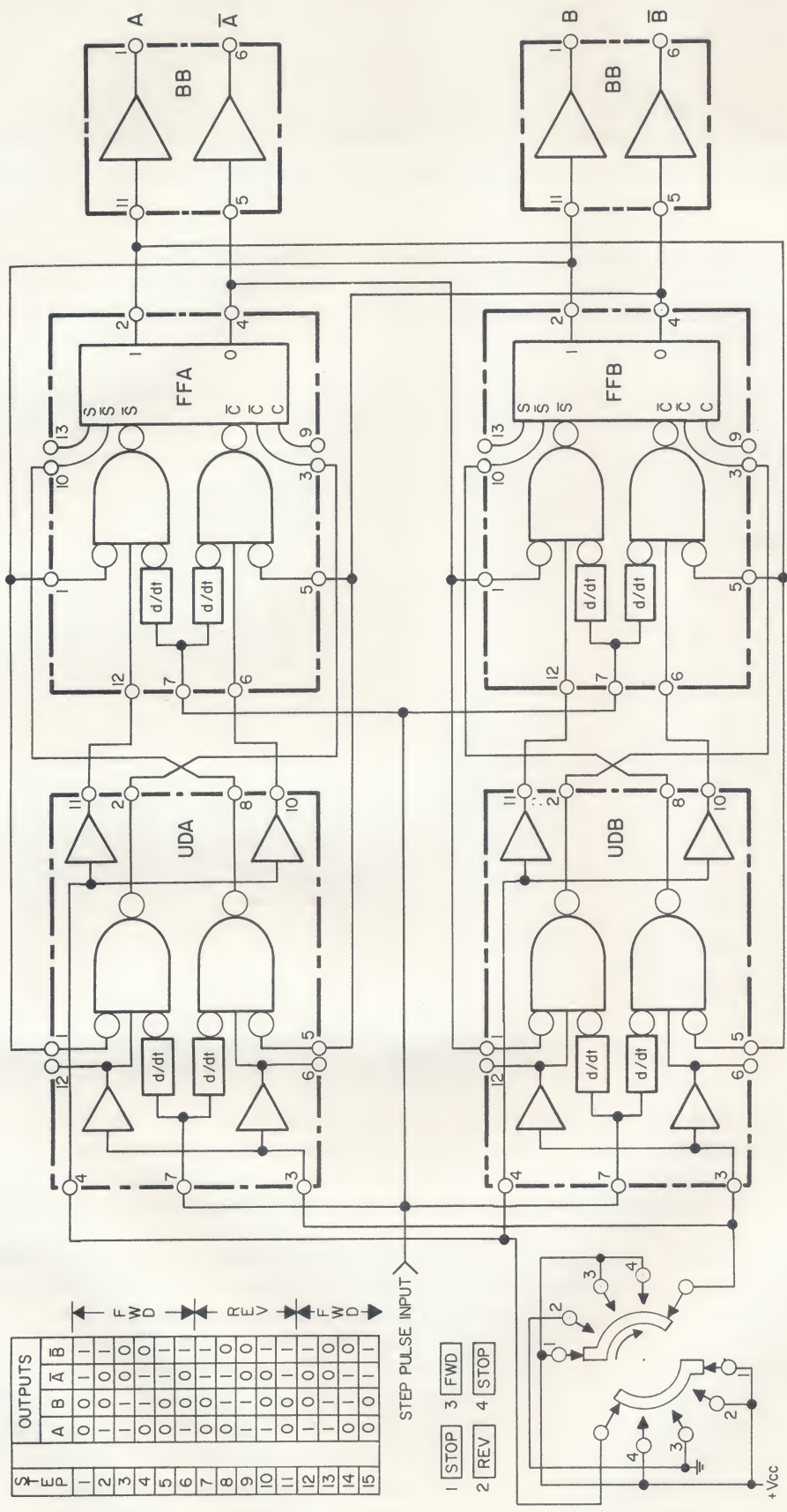


Figure 1.

Some contemporary translators perform reversal by interchanging the outputs of FFA and FFB. However, examination of the forward and reverse output tables show that in two cases out of four such practice would cause the stepping motor to step two positions in either the forward or reverse direction, thus causing an undesirable functional uncertainty.

The Intellux subsystem shown in Figure 2 performs the reversing function by causing the ring counter flip-flops to be interconnected as shown in Figure 1A or 1B automatically. For this reason, forward or reverse operation is accomplished without loss of angular reference. That is to say, when a reversal is accomplished, the stepping motor will stop on the last pulse in correspondence to its initial rotational direction and will always step in the opposite direction upon receipt of the next pulse. The automatic reversal of electrical interconnection is performed through the use of two Intellux up-down (UD) steering circuits. Control of rotation is accomplished by energizing the flip-flop (FF) steering circuits and inhibiting the UD steering circuits when forward rotation is desired, and by transposing the process when reverse direction is desired. The Table of Output States in Figure 2 illustrates an arbitrary forward-reverse sequence caused by operation of an external switch.



STEP		OUTPUTS			
		A	B	$\bar{A}$	$\bar{B}$
1	FWD	0	0	1	1
2	FWD	1	0	0	1
3	FWD	1	1	0	0
4	FWD	0	1	1	0
5	REV	0	0	1	1
6	REV	1	0	0	1
7	REV	1	1	0	0
8	REV	0	1	1	0
9	FWD	1	1	0	0
10	FWD	1	0	0	1
11	FWD	0	1	1	0
12	FWD	0	0	1	1
13	REV	1	1	0	0
14	REV	1	0	0	1
15	REV	0	1	1	0
16	REV	0	0	1	1

Figure 2. Reversible Stepping Motor Translator/Driver

The inputs for the two dual-buffers (BB) shown in Figure 2 are connected directly from the flip-flop outputs, and each buffer will provide a maximum current of 100 mA at its output.

The addition of suitable power drivers will easily provide output currents sufficient to yield motor torques in the range of 10 to 100 ounce-inches at any stepping speed of which the motors are capable.

Interconnection requirements for both the "bifilar" or "wave" type motors are shown in Figure 3. In either case, two of the motor's four windings are energized and the remaining two windings de-energized. One winding is turned OFF, and one winding is turned ON as a result of each input step pulse.

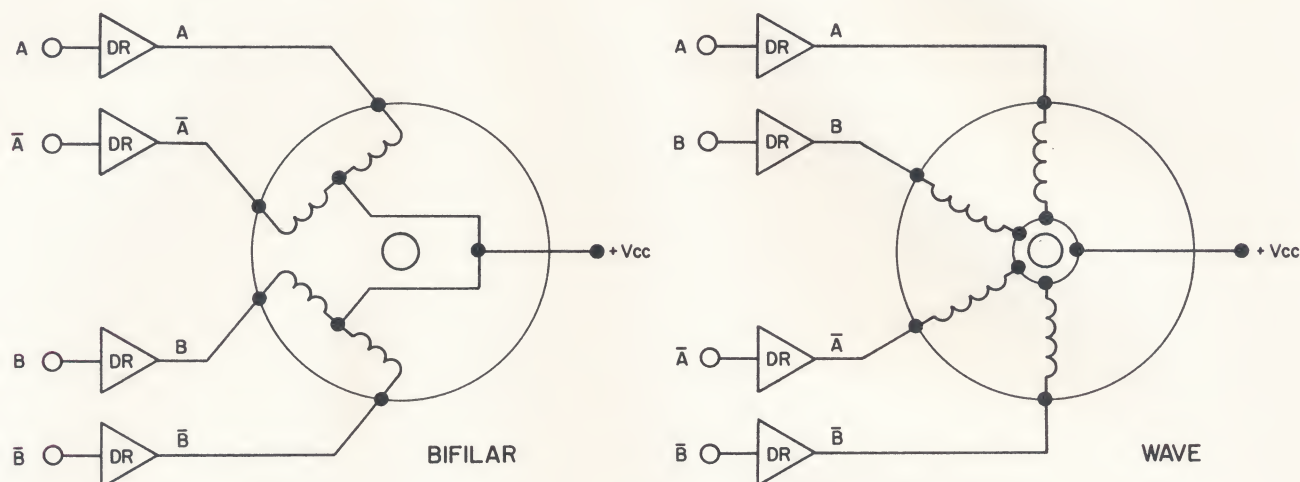


Figure 3.

A Schmitt trigger (ST) circuit may be added to sharpen the edges of incoming step pulses and provide fall times sufficiently short (200 nsec or less) to reliably clock the system.

As an additional option, a free-running multivibrator may be provided to acquire a self-clocking facility at any specified speed from ten steps per second up.

Among the advantages of Intellux's Translator/Driver system are:

Low cost -- Typically one-half the cost of contemporary Translator/Drivers.

High noise immunity -- Intellux RTL logic, which will clock at speeds to 1 MHz, provide the highest noise rejection available in standard microcircuit logic.

Simplicity of power supply -- The entire system described in this Application Note requires a single-voltage, single-polarity power supply.

Wide temperature range --

Commercial: from -22°F to $+185^{\circ}\text{F}$ (-30°C to $+85^{\circ}\text{C}$) with a single-ended power supply. Higher temperature excursions with an additional bias power supply.

Mil Spec: from -67°F to $+257^{\circ}\text{F}$ (-55°C to $+125^{\circ}\text{C}$) with bias power supply.

Back-space control -- The addition of a suitably connected, Form-C break-make, push-button, momentary-ON switch will provide the means for reversing the rotation mode, back stepping one position, and returning to the initial rotation mode each time the push-button switch is actuated.

Low Hysteresis (Adjustable) Schmitt Trigger

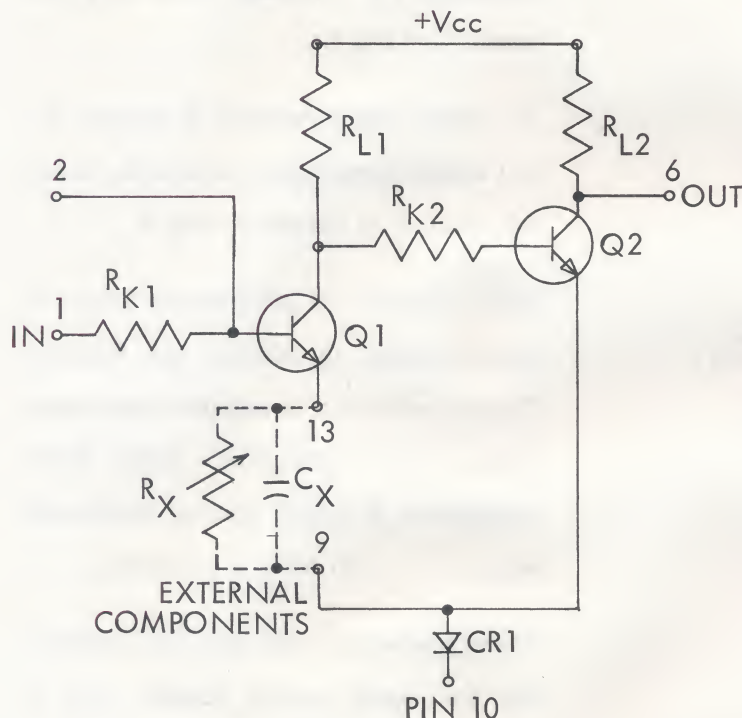


FIGURE 1. SIMPLIFIED SCHEMATIC

Intellux Schmitt Trigger hybrid microcircuits, type numbers ST2514G and ST2415G (see Fig. 1) exhibit a very low adjustable hysteresis combined with a fast fall-time output pulse.

Positive, zero, and negative hysteresis is defined in Fig. 2. Hysteresis (with pins 9 and 13 shorted) is below 50 mV for slow changes of input voltage (DC input characteristic) and is practically independent of variations in power supply voltage, V_{cc} and ambient temperature. However, hysteresis does vary

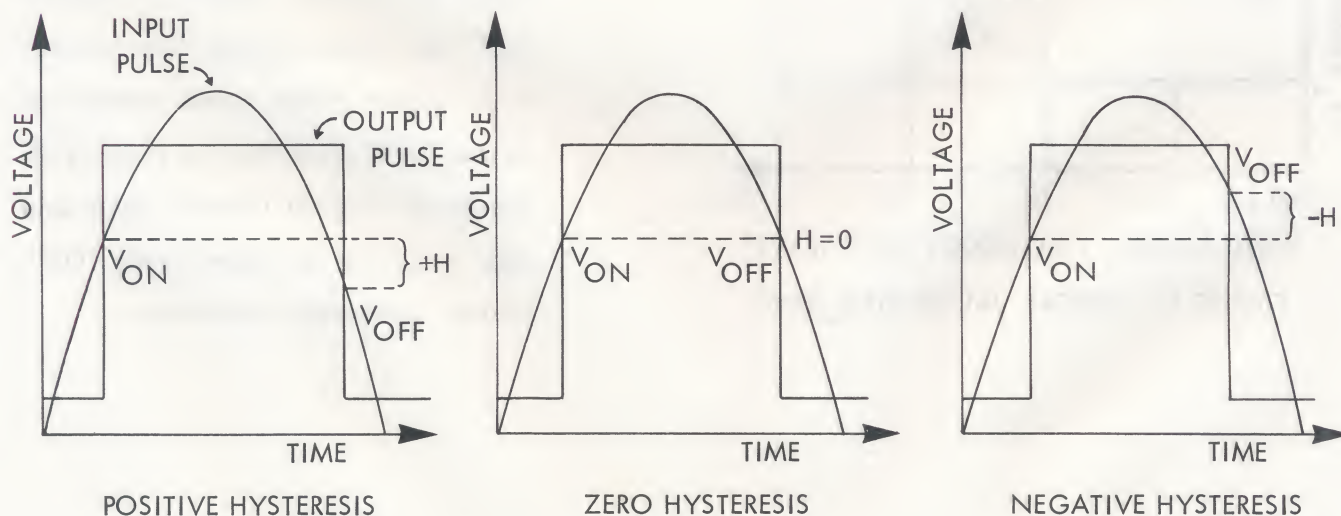


FIGURE 2. DEFINITION OF HYSTERESIS $H = V_{ON} - V_{OFF} (mV)$

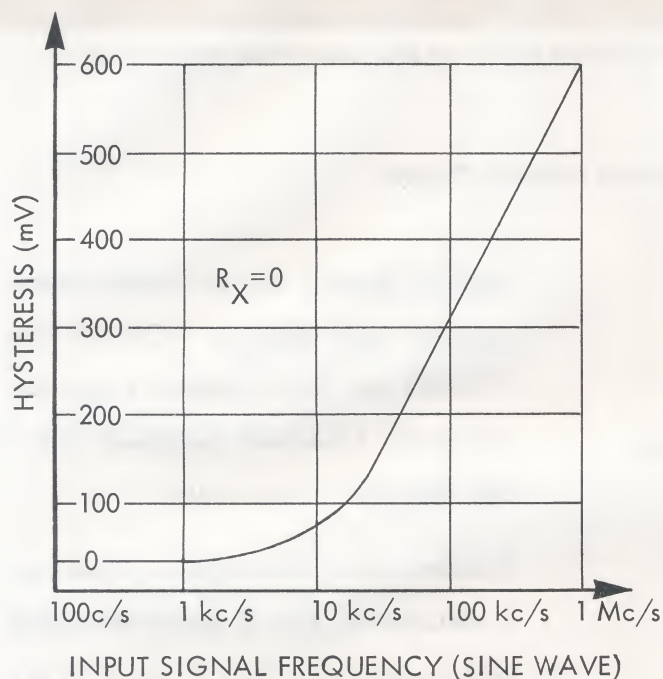


FIGURE 3. HYSTERESIS VS. FREQUENCY

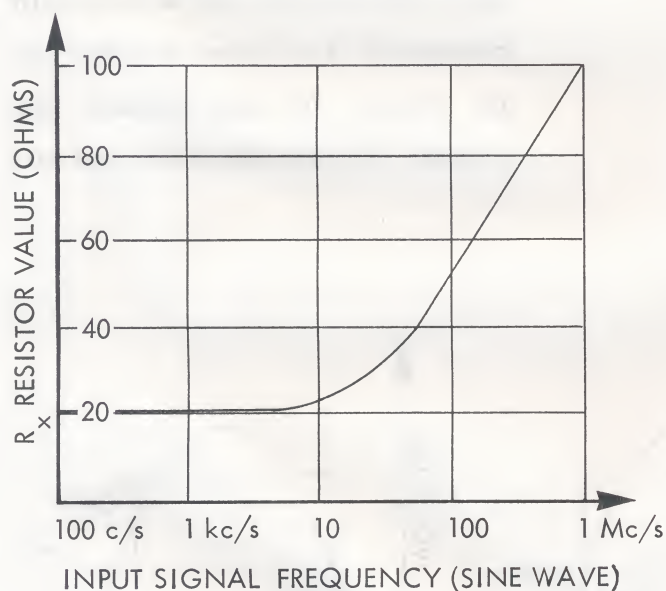


FIGURE 4. TYPICAL VALUES OF R_X (H=0)

with pulse frequency (see Fig. 3). Hysteresis can be brought to zero or a small amount negative by connecting an external resistor R_X (20 to 100 ohms) and capacitor C_X (typically 0.01 mf.) between pins 9 & 13.

To obtain zero hysteresis at various input signal frequencies, resistor R_X must be selected as shown in Fig. 4.

For a majority of applications it is not recommended to operate the Schmitt Trigger with zero or negative hysteresis values due to instability under these conditions. A small positive hysteresis (approx. 5 to 10 mV) is preferable.

When operating with very low hysteresis, the signal source should have a sufficiently low output impedance to prevent the circuit from oscillating. When the Schmitt circuit is triggered "ON" the source voltage may be lowered slightly which could switch the circuit "OFF", restoring the source voltage to its original (higher) value and thus triggering the circuit back "ON", thereby producing oscillations.

The input impedance of the Intellux Schmitt Trigger circuit is approximately 3K for the ST2514G and 2K for the ST2415G. It follows that the impedance of a signal source operating into a 10 mV hysteresis circuit should be less than 15 ohms for the ST2514G and less than 10 ohms for the ST2415G.

Typical triggering input voltage level (DC) vs. supply voltage (with pin #10 grounded) is shown in Figure 5. Figure 6 shows the variation of the triggering voltage with ambient temp. As can be seen from Fig. 6, the temperature coefficient of the triggering voltage is negative and amounts to approximately $-3 \text{ mV}/^{\circ}\text{C}$. A suitable temperature compensating circuit (e.g., thermistor-resistor type) should be connected to the base of the input transistor Q1 (pin #2) when a smaller temperature coefficient is required.

In applications where triggering of the circuit is required at input voltage levels different from the inherent values shown in Figures 5 and 6, the bias pin

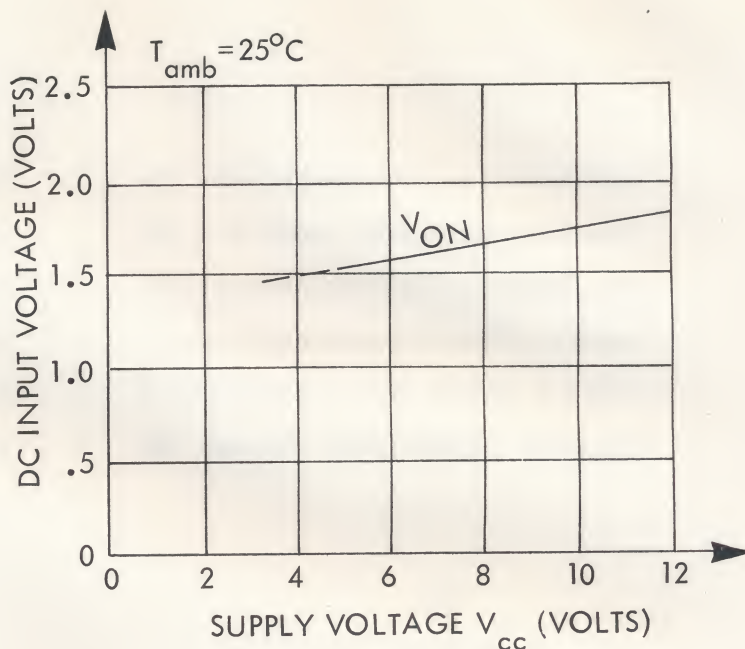


FIGURE 5. V_{ON} VS. V_{cc}

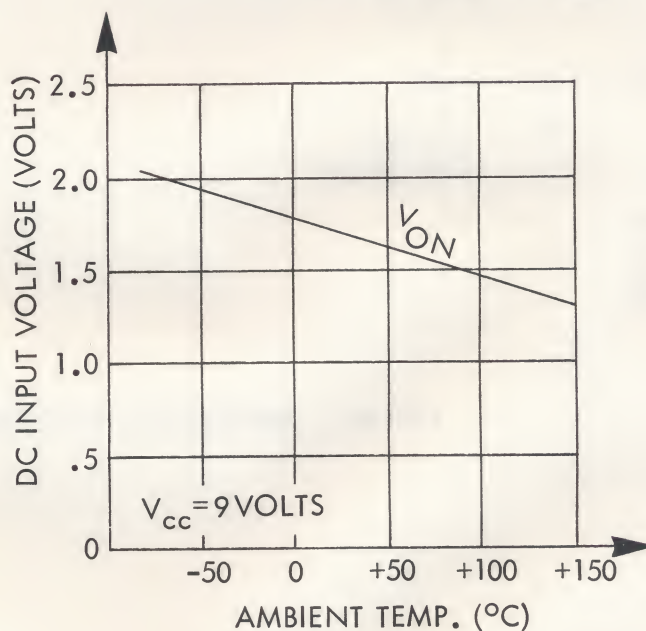


FIGURE 6. V_{ON} VS. AMBIENT TEMP.

(#10) should be connected to a low impedance power supply, such as a 10-watt Zener diode or transistorized shunt regulator. The arrangements shown in Figure 7 permit small adjustments of triggering voltage level through the

use of potentiometer R1. R1 is a vernier adjustment; large adjustments require that the Zener diode be changed. Figure 7 depicts minimal schemes; a standard, well-regulated power supply or a battery can also be used.

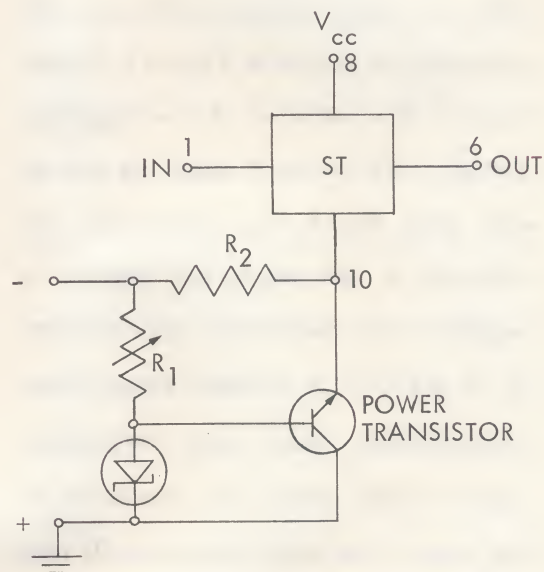
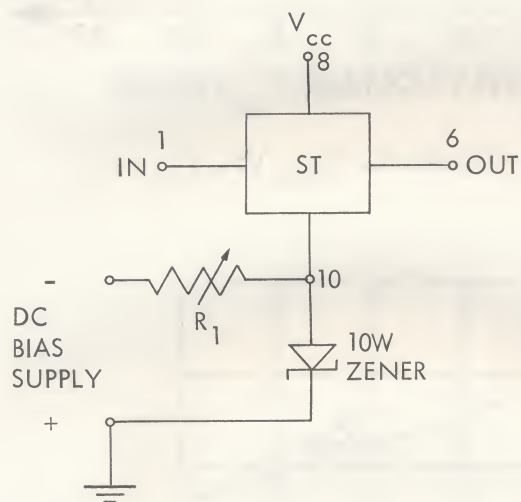


FIGURE 7. METHODS OF TRIGGERING LEVEL ADJUSTMENT

INTELLUX INCORPORATED, SANTA BARBARA RESEARCH PARK, 26 COROMAR DRIVE, GOLETA, CALIFORNIA, PHONE (805) 968-3541, CABLE: INTLUX

The SERIES M HYBRID MICROCIRCUITS are devices which are specifically designed for Aerospace systems where extreme environments and operating temperatures within the range of -55°C to $+125^{\circ}\text{C}$ are anticipated. Storage temperatures may range from -65°C to $+150^{\circ}\text{C}$.

Intellux hybrid microcircuits comprise a family of compatible digital logic and accessory circuits made up of passive thin-film and discrete semiconductor devices. Passive components are deposited on the surface of a glass substrate, hermetically sealed with one or more fused glass superstrates, and interconnected with superposed, photo-etched silver and gold-plated copper patterns. The thin film resistors and capacitors are terminated along the long edges of a $1/2'' \times 3/8'' \times 1/16''$ substrate by means of lands to which the leads of a 13-lead header are soldered. The leads are bonded to the header, which is secured to the substrate chip with epoxy resin. Therefore, the electrical connections between the passive chip components and the header leads are unaffected by thermal or mechanical stresses induced by handling or soldering of the microcircuits.

Transistors and subminiature diodes are housed within, and secured to, the glass-filled diallyl phthalate header. This provides a suitable structural form for the finished microcircuit. Transistors are provided in either TO 18 or TO 46 metal packages. The semiconductors are welded to the header leads and are thereby connected to the passive thin-film components. Since all components are hermetically sealed, there is no need for final encapsulation. However, as an added protection against moisture traps, all Intellux microcircuits are finished with an epoxy conformal coating. The completed microcircuit can be affixed to printed circuit or multilayer boards by conventional fabrication methods.

ENVIRONMENTAL DATA

Operating Temperature Range:	-55°C to $+125^{\circ}\text{C}$
Storage Temperature Range:	-65°C to $+150^{\circ}\text{C}$
Temperature Cycling:	MIL-STD 202C, Method 102A, Condition C
Moisture Resistance	MIL-STD 202C, Method 106A, Figure 106-2
Vibration, High Frequency:	MIL-STD 202C, Method 204A, Condition C
Shock, Medium Impact:	MIL-STD 202C, Method 205B, Condition C

PHYSICAL DATA

Outline Dimensions:
Standard Profile: $3/8''$ h
Low Profile: $1/4''$ h

Weight: Approximately 2 grams

Leads: Gold-plated Dumet, 0.020" diameter
x 0.300" minimum length, spaced on
0.075" centers.

Bulletin No. PD-10-66

INSTALLATION DIAGRAM

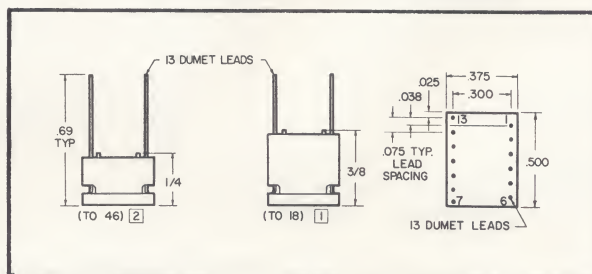


TABLE OF HYBRID MICROCIRCUIT TYPES

FLIP-FLOP TYPES	R T L			R C T L		
	Sch. No.	1/2 Std. Ω / $\square$	Std. Ω / $\square$	Sch. No.	1/2 Std. Ω / $\square$	Std. Ω / $\square$
R-S Flip-Flop	50	GG14 $\square$ 4B	GG15 $\square$ 4B	150	GG34 $\square$ 5C	GG35 $\square$ 5C
J-K Flip-Flop	40	FF24 $\square$ 4B	FF25 $\square$ 4B	140	FF44 $\square$ 5C	FF45 $\square$ 5C
T or D Flip-Flop	30	FF14 $\square$ 4B	FF15 $\square$ 4B	130	FF34 $\square$ 5C	FF35 $\square$ 5C
R/S-T or R/S-D Flip-Flop	31	FF14 $\square$ 4G	FF15 $\square$ 4G	131	FF34 $\square$ 5H	FF35 $\square$ 5H
Clamped T or Clamped D Flip-Flop	32	FF14 $\square$ 4L	FF15 $\square$ 4L	132	FF34 $\square$ 5M	FF35 $\square$ 5M

NOR/NAND GATE TYPES	R T L			R C T L		
	Sch. No.	1/2 Std. Ω / $\square$	Std. Ω / $\square$	Sch. No.	1/2 Std. Ω / $\square$	Std. Ω / $\square$
Dual 3-Input NOR/NAND Gate	50	GG14 $\square$ 4B	GG15 $\square$ 4B	150	GG34 $\square$ 5C	GG35 $\square$ 5C
5-Input NOR/NAND Gate	60	GG24 $\square$ 4B	GG25 $\square$ 4B	160	GG44 $\square$ 5C	GG45 $\square$ 5C
3-Input Buffered NOR/NAND Gate	10	GB14 $\square$ 4B	GB15 $\square$ 4B	110	GB24 $\square$ 5C	GB25 $\square$ 5C
3-Input NOR/NAND Gate and Buffer	11	GB14 $\square$ 4G	GB15 $\square$ 4G	111	GB24 $\square$ 5H	GB25 $\square$ 5H

ACCESSORY CIRCUIT TYPES	Sch. No.	Type No.	Remarks
Steering Circuit (For up-down counting)	90	UD14 $\square$ 4B	For use with FF14 $\square$ 4B
	90	UD15 $\square$ 4B	For use with FF15 $\square$ 4B
	190	UD24 $\square$ 5C	For use with FF34 $\square$ 5C
	190	UD25 $\square$ 5C	For use with FF35 $\square$ 5C
Delay Multivibrator	22	DM44 $\square$ 0B	Short delay (100 nsecs to 100 usecs)
	23	DM35 $\square$ 0B	Medium delay (10 usecs to 10 msecs)
	23	DM37 $\square$ 0B	Long delay (100 usecs to 1 second)
Schmitt Trigger	83	ST24 $\square$ 5L	High speed squaring (5 MHz typical)
	83	ST25 $\square$ 4L	Medium speed squaring (1 MHz typical)
	81	ST24 $\square$ 5B	ST24 $\square$ 5L with isolated bias
	81	ST25 $\square$ 4B	ST25 $\square$ 4L with isolated bias
Current Driver	1	CD15 $\square$ 4B	For loads to 100 mA
	1	CD14 $\square$ 4G	For loads to 330 mA
Dual Relay Driver	74	RD15 $\square$ 3BD	For loads to 100 mA @ 15 volts max.
	74	RD14 1 3ND	For loads to 330 mA @ 30 volts max.

$\square$ Note: Blank square in type numbers reserved for profile designator; Number 1 indicates Standard Profile, Number 2 indicates Low Profile. Example:
 ST2415L = High Speed Schmitt Trigger; Standard Profile
 ST2425L = High Speed Schmitt Trigger; Low Profile

LOGIC MICROCIRCUITS

QUANTITY	1-25	26-50	51-100	101-500	501-1000
J-K FLIP-FLOP					
FF2414B	14.75	12.50	10.65	9.50	8.50
FF2514B	14.75	12.50	10.65	9.50	8.50
FF4415C	19.75	16.75	14.25	12.75	11.40
FF4515C	19.75	16.75	14.25	12.75	11.40
TRIGGER OR DELAY FLIP-FLOP					
FF1414B	14.75	12.50	10.65	9.50	8.50
FF1514B	14.75	12.50	10.65	9.50	8.50
FF3415C	19.75	16.75	14.25	12.75	11.40
FF3515C	19.75	16.75	14.25	12.75	11.40
R/S-T OR R/S-D FLIP-FLOP					
FF1414G	15.75	13.50	11.65	10.50	9.50
FF1514G	15.75	13.50	11.65	10.50	9.50
FF3415H	20.75	17.75	15.25	13.75	12.40
FF3515H	20.75	17.75	15.25	13.75	12.40
CLAMPED-T OR CLAMPED-D FLIP-FLOP					
FF1414L	16.75	14.50	12.65	11.50	10.50
FF1514L	16.75	14.50	12.65	11.50	10.50
FF3415M	21.75	18.75	16.25	14.75	13.40
FF3515M	21.75	18.75	16.25	14.75	13.40
DUAL 3-INPUT NOR/NAND GATE OR R-S FLIP-FLOP					
GG1414B	12.50	10.60	9.00	8.10	7.30
GG1514B	12.50	10.60	9.00	8.10	7.30
GG3415C	16.75	14.20	12.10	10.85	9.80
GG3515C	16.75	14.20	12.10	10.85	9.80
5-INPUT NOR/NAND GATE					
GG2414B	12.50	10.60	9.00	8.10	7.30
GG2514B	12.50	10.60	9.00	8.10	7.30
GG4415C	16.75	14.20	12.10	10.85	9.80
GG4515C	16.75	14.20	12.10	10.85	9.80
3-INPUT BUFFERED NOR/NAND GATE					
GB1414B	13.50	11.60	10.00	9.10	8.30
GB1514B	13.50	11.60	10.00	9.10	8.30
GB2415C	17.75	15.20	13.10	11.85	10.80
GB2515C	17.75	15.20	13.10	11.85	10.80
3-INPUT NOR/NAND GATE & BUFFER					
GB1414G	13.50	11.60	10.00	9.10	8.30
GB1514G	13.50	11.60	10.00	9.10	8.30
GB2415H	17.75	15.20	13.10	11.85	10.80
GB2515H	17.75	15.20	13.10	11.85	10.80

(Ordering data on reverse side)

ACCESSORY MICROCIRCUITS

QUANTITY	1-25	26-50	51-100	101-500	501-1000
STEERING CIRCUIT					
UD1414B	15.75	13.40	11.40	10.25	9.25
UD1514B	15.75	13.40	11.40	10.25	9.25
UD2415C	18.75	15.95	13.55	12.20	11.00
UD2515C	18.75	15.95	13.55	12.20	11.00
DELAY MULTIVIBRATOR					
DM4410B	15.75	13.40	11.40	10.25	9.25
DM3510B	17.25	14.65	12.50	11.25	10.15
DM3710B	18.75	15.95	13.55	12.20	11.00
SCHMITT TRIGGER					
ST2415L	15.75	13.40	11.40	10.25	9.25
ST2514L	15.75	13.40	11.40	10.25	9.25
ST2415B	15.75	13.40	11.40	10.25	9.25
ST2514B	15.75	13.40	11.40	10.25	9.25
CURRENT DRIVER					
CD1514B	15.75	13.40	11.40	10.25	9.25
CD1414G	18.75	15.95	13.55	12.20	11.00
DUAL RELAY DRIVER					
RD1513BD	15.75	13.40	11.40	10.25	9.25
RD1413ND	18.75	15.95	13.55	12.20	11.00

ORDERING DATA

DELIVERY:	All items generally available from stock.
TERMS:	Net 30 days.
F.O.B.	Goleta, California
MIXED LOT:	Special pricing for mixed lots in excess of 500 pcs.
VOLUME PRICING:	Pricing from manufacturer for quantities in excess of 1000 pcs.

NOTE

All prices are for standard profile. Add premium of \$1.00 for low profile.

HYBRID MICROCIRCUIT NOISE IMMUNITY

The purpose of this bulletin is to provide the users of Intellux products with specific information on noise immunity as it applies to gates. Only input noise will be considered. The Intellux gates to be discussed will be considered from two standpoints:

1. Those equipped with speed-up capacitors such as Intellux Gate GG3317E (RCTL)
2. Those without speed-up capacitors such as Intellux Gate GG1514B (RTL)

Definitions*

A **noise signal** is defined as an unprogrammed, externally-generated electrical signal that enters the operating gate. If large enough, it may upset the programmed logic signal passing through the gate. the **noise immunity** of the gate is defined as the largest amplitude (in volts) of a normalized noise signal that will not upset the logic state of the gate.

Basic Rules

1. A noise signal (normalized) with an amplitude less than the noise immunity value, will be attenuated to zero when passing thru a cascaded chain of gates.
2. When the noise signal is larger than the noise immunity value, it will be amplified in a chain of gates and will eventually reach a value large enough to act as an actual input signal, thus interfering with the programmed signal.
3. When a system involves gates and flip-flops, the lower-valued noise immunity is the one that applies for the entire system.
4. A noise signal can enter the gate circuit via the input connection or any other connection that may be capable of picking up externally generated signals (i.e., power supply connection, ground connection, etc.)
5. The noise immunity value in any one gate differs considerably depending on the path taken by the noise signal. In the data to follow, direct figures are given for the **input** noise immunity only.
6. The value of the noise immunity of a gate depends on its logic state. Thus, two generally different values are necessary to describe the noise immunity of the gate. One value, the "O-state noise immunity," applies to the gate in the O-state and positive noise pulses, while the second value is the "1-state noise immunity" and applies to the gate in the 1-state and negative noise pulses.

*See also "Noise Margins in Digital Integrated Circuits," Proceedings of the IEEE Volume 52, No. 12, p 1565.

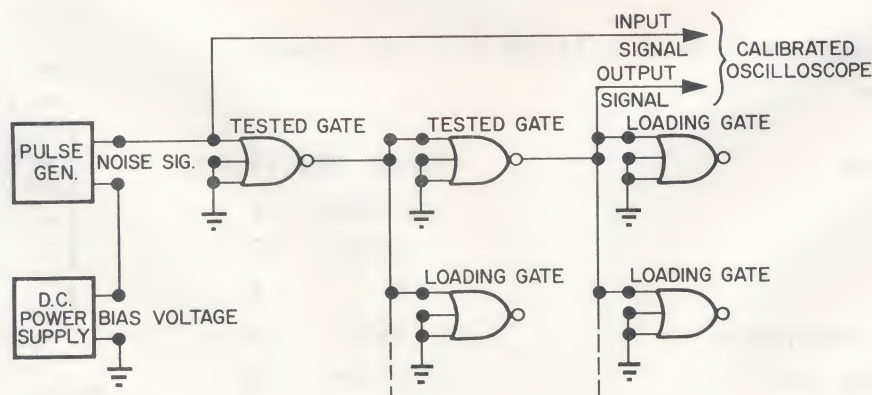


FIG. 1.

TEST METHODS AND RESULTS

The tested gates were connected as shown in Figure 1. The following parameters were monitored:

Table 1

Parameter	Gate	
	GG1514B	GG3317E
Power supply voltage, V_{cc} , volts	9	6
Bias voltage, V_{bb} , volts	0	0
Fanout, N	3	3
Ambient Temperature, T_a , °C	25	25
Noise pulse width, W_p	1 μ sec	500 nsec

A large number of Intellux Hybrid Microcircuits were tested using the preceding normalized conditions. The average value of normalized noise immunity for Intellux Gates GG1514 B and GG3317E is as shown in Table 2.

Table 2

State	Gate	
	GG1514B	GG3317E
"0" state noise immunity, volts	2.2	2.1
"1" state noise immunity, volts	3.0	1.2

HOW TO USE THE CURVES

To obtain the correct noise immunity figure for any set of conditions different from the normalized conditions, multiply the normalized value by the appropriate multipliers as shown in Figures 2 thru 6 for GG1514B and Figures 7 thru 11 for GG3317E.

EXAMPLE

Find the noise immunity of GG1514B under the following conditions:

CONDITION	VALUE	SEE FIGURE
V_{cc}	12 volts	2
V_{bb}	-3 volts	3
Fanout	5	4
Ambient temperature	-55°C	5
Noise pulse width	.2 μ sec	6

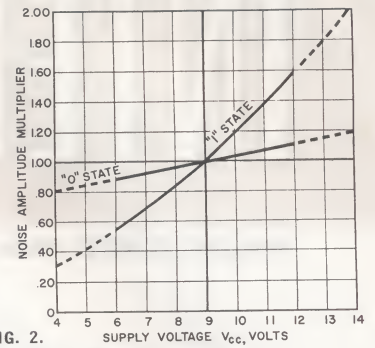


FIG. 2.

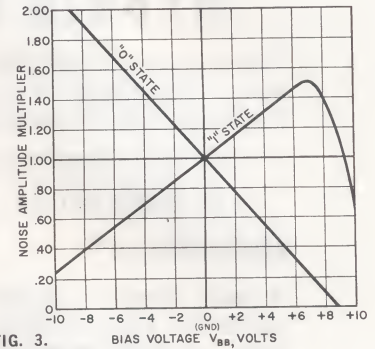


FIG. 3.

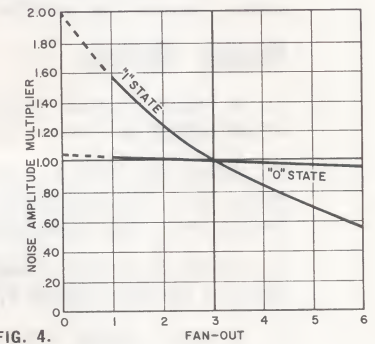


FIG. 4.

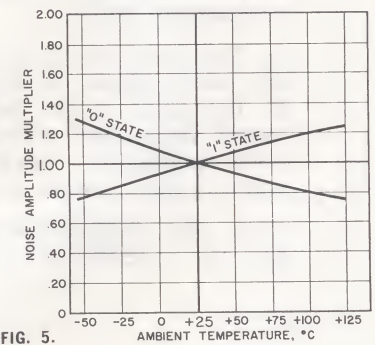


FIG. 5.

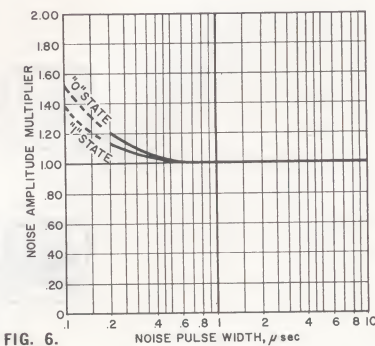


FIG. 6.

From the curves of Figures 2 thru 6 are found the following values for the "0" state:

CONDITION	NOISE IMMUNITY MULTIPLIER
V_{cc}	1.10
V_{bb}	1.33
Fanout	0.97
Ambient Temperature	1.30
Noise pulse width	1.20

Now, using the "0" state immunity for GG1514B as shown in Table 2 (2.2) and multiplying all values:

$$2.2 \times 1.10 \times 1.33 \times 0.97 \times 1.30 \times 1.20 = 4.87$$

Thus, the "0" noise immunity value in volts for GG1514B under the selected conditions is

4.87 volts

To find the noise immunity value for the "1" state:

CONDITION	NOISE IMMUNITY MULTIPLIER
V_{cc}	1.58
V_{bb}	0.76
Fanout	0.69
Ambient temperature	0.78
Noise pulse width	1.15

Now using the "1"-state immunity for GG1514B as shown in Table 2 (3.0) and multiplying all values:

$$3.0 \times 1.58 \times 0.76 \times 0.69 \times 0.78 \times 1.15 = 2.23$$

Thus, the "1"-state noise immunity value in volts for GG1514B under the selected conditions is

2.23 volts

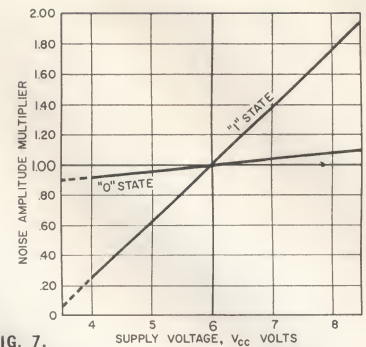


FIG. 7.

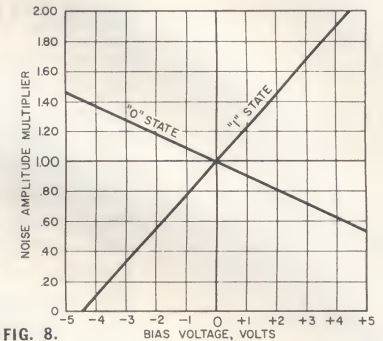


FIG. 8.

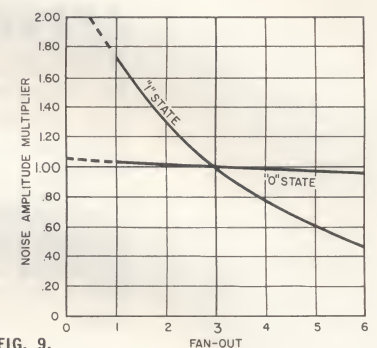


FIG. 9.

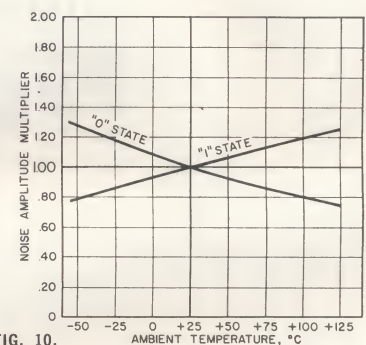


FIG. 10.

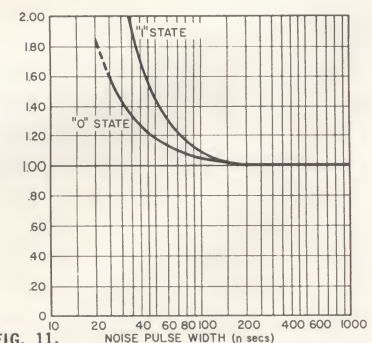


FIG. 11.

DISCUSSION OF RESULTS

An examination of the multiplier curves reveals that the noise immunity increases with the supply voltage and decreases with the fanout. It also increases with narrower pulse width. For very wide pulse width, the noise immunity figure equals the dc noise immunity. Changes in ambient temperature affect differently the noise immunity for the two states. Noise immunity in the "0" state decreases with the ambient temperature, while noise immunity in the "1" state increases with ambient temperature. The bias voltage also has a different influence on the two states. Making the bias voltage more negative will increase the "0" state immunity but will decrease the "1" state noise immunity.

APPLICATION NOTES

If the calculated noise immunity for the "0" state is too low, it can be improved by applying some negative bias (Fig. 3). The same bias will, however, reduce the noise immunity for the "1" state. A compromise has to be reached to decide the appropriate value of the bias voltage.

It is apparent from the figures that the noise immunity of the gate without the speed-up capacitor (GG1514B) is higher than the noise immunity with the speed-up capacitor (GG3317F). When maximum noise immunity is required, the slower type (GG1514B) should be used.

SUMMARY AND CONCLUSIONS

One of the fundamental advantages of the digital techniques is that it has the inherent capability of high noise immunity. As demonstrated in the preceding pages, Intellux gates possess excellent noise immunity. This advantage may be obtained in either the military or commercial units.